AMENDMENTS TO THE CLAIMS

Listing of Claims

A listing of the entire set of pending claims is submitted herewith per 37 CFR 1.121. This listing of claims will replace all prior versions, and listings, of claims in the application.

1-13. (cancelled)

14. (currently amended) Electrical circuit arrangement [[(A)]] for a display device [[(6)]], the electrical circuit arrangement [[(A)]] comprising

an input terminal ~~(11;13)~~ for receiving a first signal ~~(I_{prog}; I_{dat})~~;

a first memory element ~~(M1)~~ for storing information ~~about~~ related to the first signal ~~(I_{prog}; I_{dat})~~;

a second memory element;

a driver element [[(D)]] coupled to the first memory element ~~(M1)~~ for outputting a second signal ~~(I_{light}; I_{prog})~~ via an output terminal ~~(15;11) in accordance with~~ based on the information about the first signal; and

a calibration circuit [[(S)]] coupled between the driver element [[(D)]] and the input terminal ~~(11;13)~~ for matching a potential difference between the driver element [[(D)]] and the input terminal ~~(11;13)~~ during a calibration phase prior to receiving the first signal ~~(I_{prog};I_{dat})~~, the matching being such that there is no voltage change required at the input terminal ~~(11;13)~~ during a subsequent programming phase if during ~~this~~ a current programming phase the second signal ~~has to be~~ is programmed to the same value as during ~~the~~ a previous programming phase,

wherein the calibration circuit comprises a calibration transistor coupled with a main terminal between the input terminal and the driver element, and

wherein the second memory element is coupled to a gate of the calibration transistor.

15. (currently amended) Electrical circuit arrangement [[(A)]] according to claim [[15]] 14, the calibration circuit [[(S)]] comprising a calibration switch ~~(S_{cal})~~ for coupling the input terminal ~~(11;13)~~ to a calibration voltage ~~(V_{cal})~~.

16. (cancelled)

17. (currently amended) Electrical circuit arrangement [[(A)]] according to claim [[17]] 14, wherein the second memory element ~~(M2) being adapted~~ is configured for storing data related to the first signal ~~(I_{prog}; I_{dat})~~ obtained from the first memory during the calibration phase.

18. (currently amended) Electrical circuit arrangement [[(A)]] according to claim [[17]] 14, the calibration circuit [[(S)]] further comprising a first switch ~~(S5)~~ coupled between one of the main terminals and the gate of the calibration transistor ~~(T_{cal})~~.

19. (currently amended) Electrical circuit arrangement [[(A)]] according to claim [[15]] 14, comprising a ~~further~~ second switch [[(S3)]] coupled between the driver element [[(D)]] and the output terminal ~~(15;11)~~.

20. (currently amended) Electrical circuit arrangement [[(A)]] according to claim [[15]] 14, comprising a third switch ~~(S1)~~ coupled between the driver element [[(D]]) and the calibration circuit [[(S)]].

21. (currently amended) Electrical circuit arrangement [[(A)]] according to claim [[15]] 14, wherein said driver element (D) is a drive transistor ~~(T2)~~ having a gate connected to said first memory element ~~(M1)~~, and a main terminal coupled to the calibration circuit [[(S)]], said gate further being coupled via a fourth switch ~~(S4)~~ to the main terminal of the drive transistor ~~(T2)~~.

22. (cancelled)

23. (currently amended) Display device [[(6)]] comprising:

a plurality of display pixels [[(3)]], each of the display pixels [[(3)]] comprising an electrical circuit arrangement (A) according to claim [[15]] 14, and an emissive element ~~(14)~~ coupled to said output terminal ~~(15)~~ and adapted to emit light on reception of said second signal ~~(I_{light})~~; and

a display controller [[(7)]] adapted to control the calibration phase of the plurality of display pixels [[(3)]].

24. (currently amended) Display device [[(7)]] according to claim [[24]] 23, comprising for each input terminal ~~(11;13)~~ one common calibration switch ~~(S_{cal})~~ for coupling the input terminal ~~(11;13)~~ to a calibration voltage ~~(V_{cal})~~.

25-26. (cancelled)

27. (currently amended) Method for addressing a display pixel [[(3)]] of a display device [[(6)]] comprising an input terminal ~~(11),~~ a first memory element ~~(M1; C)~~, a second memory element ~~($M2; C_{cal}$)~~, a driver transistor ~~(T2)~~ coupled to an output terminal ~~(15)~~, and a calibration circuit [[(S)]] comprising a calibration transistor coupled with a main terminal between the driver transistor ~~(T2)~~ and the input terminal ~~(11)~~, wherein the second memory element is coupled to the calibration transistor, the method comprising the steps of:

storing information about a first signal ~~(I_{prog})~~ in said first memory element ~~(C)~~;

generating a second signal ~~(I_{light})~~ from said driver transistor ~~(T2)~~ in accordance with the information about the first signal ~~(I_{prog})~~; and

enabling the calibration circuit [[(S)]] to match a potential difference between the driver transistor ~~(T2)~~ and the input terminal ~~(11)~~ during a calibration phase prior to receiving the first

signal ~~(I_{prog})~~, the matching being such that there is no voltage change required at the input terminal ~~(11)~~ during a subsequent programming phase if during this programming phase the second signal has to be programmed to the same value as during the previous programming phase.

28. (new) An electrical circuit arrangement for a display device, comprising:

an input terminal for receiving a first signal;

a first memory element for storing information about the first signal;

a driver transistor having a main terminal and a gate connected to the first memory element for outputting a second signal via an output terminal based on the information about the first signal, wherein the gate is further coupled via a switch to the main terminal; and

a calibration circuit coupled between the main terminal and the input terminal for matching a potential difference between the driver transistor and the input terminal during a calibration phase prior to receiving the first signal, the matching being such that there is no voltage change required at the input terminal during a subsequent programming phase if during a current programming phase the second signal is programmed to the same value as during a previous programming phase.